

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-8 are pending in the present application. Claims 1, 2, 7, and 8 are amended by the present amendment.

In the outstanding Office Action, Claims 1-8 were rejected under 35 U.S.C. § 112, first paragraph, and Claims 1-8 were rejected under 35 U.S.C. § 103(a) as unpatentable over Ooishi (U.S. Patent No. 6,914,845) in view of Lutkemeyer (U.S. Patent No. 6,879,196).

In view of the rejection of Claims 1-8 under 35 U.S.C. § 112, first paragraph, independent Claims 1 and 8 have been amended to recite that a second circuit and not a first circuit has a normal operation state and a standby state, as suggested by the outstanding Office Action. No new matter has been added. Accordingly, it is respectfully submitted this rejection be withdrawn.

In view of the outstanding grounds for rejection on the merits, independent Claims 1 and 8 have been amended to more clearly recite first, second, and third clock generators and various relationships among these clock generators and their signals. The claim amendments find support in Figure 2 and its corresponding description in the specification. No new matter has been added.

Briefly recapitulating, amended Claim 1 is directed to an electronic apparatus that has a first circuit and a second circuit. The second circuit has a normal operation state and a standby state. First and second clock generators are disposed in the first circuit and are configured to generate first and second clock signals. A third clock generator is disposed in the second circuit and is configured to generate a third clock signal. The second clock signal is provided to the first circuit and the second circuit, and the third clock generator generates the third clock signal only when the third clock generator received the second clock signal.

In a non-limiting example, Figure 2 shows the first circuit 21, the second circuit 22, the first clock generator 10, the second clock generator 20, and the third clock generator 50.

The claimed electronic apparatus advantageously reduces a power consumption in a standby state as described in the specification at page 4, line 24, to page 5, line 7.

Turning to the applied art, Ooishi shows in Figure 1 a power control unit that activates a control signal ST for a circuit block to be set to a standby state before turning off power of the circuit block.¹ However, as recognized by the outstanding Office Action at page 4, first full paragraph, “Ooishi does not disclose about clock controlling means for controlling generation of a first clock and a second clock.”

To cure this deficiency, the outstanding Office Action relies on Lutkemeyer, which discloses a method for providing a signal delay compensation for circuits such as a multi-pair gigabit Ethernet transceiver. In this respect, Lutkemeyer shows in Figure 1 a timing circuit 20 that includes a master clock 44 and a delay adjuster 24, which maintains “phase synchronization between clocks 26 and 28.”²

However, neither Lutkemeyer nor Ooishi teaches or suggests first and second clock generators disposed in a first circuit and a third clock generator disposed in a second circuit, and the third clock generator generating the third clock signal only when the third clock generator receives the second clock signal as required by amended Claims 1 and 8.

Accordingly, it is respectfully submitted that independent Claims 1 and 8 and each of the claims depending therefrom patentably distinguish over Ooishi and Lutkemeyer, either alone or in combination.

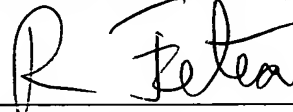
¹ Ooishi, see Abstract.

² Lutkemeyer, column 3, lines 31-37.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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